'a6 Cont'd.

· a third adder which outputs an output signal by adding the first corrected signal and the second corrected signal.--

REMARKS

Claims 1-31 are pending in the application. The allowance of claim 12 and the indication that dependent claims 4, 5, 10 and 26 would be allowable if rewritten in independent form are noted with appreciation. Allowable claims 4, 5 and 10 are being rewritten in independent form since their parent claims are being amended, and desired to so amend the allowable claims. Allowable claim 26 is not being rewritten in independent form since its parent claims are not being amended. Independent claims 1, 13 and 28 are also being amended. New claims 30 and 31 are being added. Favorable reconsideration of the application, as amended, is respectfully requested.

Claims 1-3, 6, 8, 9, 11, 13-19, 25, 27 and 28

Claims 1-3, 6, 8, 9, 11, 13-19, 25, 27 and 28 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. patent no. 4,766,495 of Kobayashi et al. This rejection is respectfully traversed for at least the following reasons.

Kobayashi et al. describes a circuitry for correcting the phase of an input sampled signal having discrete digital data. As shown in Figures 6 and 7, the primary objective of Kobayashi et al. is to interpolate the phase error signal SVE based on the equation (2), DINj = k1 D0N + k2 D0(N+1) (j=0, 1, 2, 3, 4), where k1 and k2 are weighting coefficients, and D0N and D0(N+1) are sampled data. (column 5, line 36 - column 6, line 16.) The sampled data D0N and D0(N+1) are multiplied by k1 and k2, respectively.

Claim 1 of the present application, on the other hand, is directed to a hue signal correction circuit having a digital filter and a correction signal input. Specifically, as illustrated in Figure 4 of the present specification, the coefficient circuitry 76 adds the differential signal output 63 and the correction value 74, and outputs the added signal.

Claims 1, 13, 18 and 28 recite adding the correction signal to the input signal. Kobayashi et al. fails to teach or suggest adding the correction signal to the input signal. For example, in Figure 5, the multipliers 24 and 26 multiply the sampled data D0N and D0(N+1) by the weighting coefficients k1 and k2. This multiplying operation of Kobayashi et al. is

LAW OFFICES OF
SKJERVEN, MORRILL,
MACPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

clear from the equation (2), DINj = k1 D0N + k2 D0(N+1). Thus, Figure 5 fails to disclose addition of the correction signal of the present invention.

Nor does Figure 8 of Kobayashi et al. teach or suggest adding the correction signal. Figure 8 also shows the multipliers 36-40, which multiplies the sampled data D0(N+4), D0(N+3), D0(N+2), D0(N+1) and D0N, respectively, but does not show an addition circuit which adds a correction signal to an input signal in any way.

Therefore, Kobayashi et al. do not teach or suggest each and every element of claims 1, 13, 18 and 28. Moreover, Kobayashi et al. do not teach or suggest the advantage associated with the invention as claimed. For example, the Kobayashi et al. apparatus is more prone to overcorrect the input signal, while the present invention is capable of keeping the hue signal bounded.

The rejected claims dependent from claims 1, 13, 18 and 28 not specifically mentioned herein are also considered to be patentably distinguishable over Kobayashi et al. For example, such claims are distinguishable for at least the same reasons stated above in connection with the independent claims from which they depend.

Withdrawal of the rejection under 35 U.S.C. 102(b) of claims 1-3, 6, 8, 9, 11, 13-19, 25, 27 and 28 is respectfully requested.

Claims 21-24

Claims 21-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kobayashi et al. This rejection is respectfully traversed for at least the following reasons.

Claims 21-24 depend, directly or indirectly, from claim 18. Consequently, these claims are believed to be allowable for at least the same reasons stated above in connection with claim 18. In addition, however, the Examiner has failed to establish a prima facie case of obviousness since the Examiner has rejected the claims over a the Kobayashi et al. reference alone without citing any evidence to support the allegation that the differences between claims 21-24 and the Kobayashi et al. reference would have been obvious.

Regarding claim 21, the applicant respectfully disagrees with the Examiner and requests the Examiner to provide an evidence that the preset range of zero to 2π would have been well known in the art. Also, regarding claim 22, the applicant respectfully disagrees with the Examiner and requests, if this rejection is maintained, that evidence be supplied that shows the preset range of zero to 2π plus a guard band would have been well known in the art.

LAW OFFICES OF
SKJERVEN, MORRILL,
MACPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Regarding claim 23, the Examiner does not state the reason why the guard band having a reference value above or below the range zero to 2π would have been obvious. The applicant respectfully requests the Examiner to state the reason for the purported obviousness, if this rejection is maintained.

Regarding claim 24, the Examiner again does not state the reason why the guard bands having $-\pi$ to zero and 2π to 3π would have been obvious. If this rejection is maintained, further evidence supporting the conclusion of obviousness is requested.

Claims 7, 20 and 29

Claims 7, 20 and 29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kobayashi et al. in view of U.S. patent no. 5,381,238 to Namiki et al. This rejection is respectfully traversed for at least the following reasons.

Claims 7 and 20 depend from claims 1 and 18, respectively. Consequently, these claims are believed to be allowable for at least the same reasons stated above in connection with claims 1 and 18. In addition, regarding claim 7, Namiki et al. fail to teach or suggest the adjustment input causing an integer multiple of 2π shift since the phase shifters 91-94 of Namiki et al. are not the "second circuit portion" of claim 1 which "adds the adjustment input to the delayed signal input." Furthermore, the phase shifters 91-94 of Namiki et al. shift phases by 0, 90, 180, 270 degrees, respectively, which are an integer multiple of π shift, not 2π shift as recited in claim 7. Thus, with respect to claim 7, Namiki et al. do not make up the deficiencies of Kobayashi et al. in any way. Accordingly, claim 7 is patentable over Kobayashi et al. and Namiki et al., individually or in combination.

Claim 20 recites the correction signal of an integer multiple of 2π in a similar way to that of claim 7. Therefore, claim 20 is patentable over either of the Kobayashi et al. or Namiki et al. patents, individually or in combination, for at least the same reasons as set forth above in connection with claim 7.

Claim 29 recites the filtered hue information signal which includes unfiltered offsets. However, Namiki et al. fail to teach or suggest the "offset" recited in claim 29 since the phase shifters 91-94 in Figure 15 of Namiki et al. do not generate any "offset" signal. Rather, Namiki et al. shift the phase of the input signal instead of adding the unfiltered offsets signal to the filtered hue information signal. Therefore, again, Namiki et al. do not make up the deficiencies of Kobayashi et al. Accordingly, claim 29 is submitted to be patentable over Kobayashi et al. and Namiki et al. individually or in combination.

LAW OFFICES OF
SKJERVEN, MORRILL,
MACPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

New Claims 30 and 31

New claims 30 and 31 have been added to define further the invention. Claim 30 recites adding the unfiltered offsets to the hue information signal, and claim 31 recites the first adder which adds the correction signal to the input signal. As set forth above in connection with claims 1, 13, 18 and 28, neither Kobayashi et al. nor Namiki et al. disclose the addition of the correction signal to the input signal as recited in claims 30 and 31. Therefore, claims 30 and 31 are believed to be allowable for at least the reasons similar to those pointed out above in connection with claims 1, 13, 18 and 28.

Conclusion

For at least the above reasons, all claims pending in the application are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate the prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on Dec. 13, 2000.

Brenda J. Dolly — Date of Signature: 12/13/00

Respectfully submitted,

Gerald P. Parsons — Date: 12/13/00

Gerald P. Parsons
Attorney for Applicant
Reg. No. 24,486

LAW OFFICES OF
SKJERVEN, MORRILL,
MACPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979